DATA SHEET
UFQ8HSR8
OSFP 800G SR8 Transceiver(MMF,8x100G PAM4 850nm 100m Dual MPO-12 APC)

PRODUCT FEATURES

Part Number	Product Description
UFQ8HSR8	OSFP 800G SR8 Transceiver(MMF,8x100G PAM4 850nm 100m Dual MPO-12 APC)

Product Features

- Hot-pluggable OSFP form factor
- 8x100G PAM4 retimed 800GAUI-8 electrical interface
- Dual MPO-12 APC connector and MPO16 APC connector are provided
- 8 channel VCSEL arrays and 8 channels PIN photo detector arrays
- Maximum link length of 60m on OM3 or 100m on OM4
- Compliant to OSFP Module Specification Rev 5.0
- Compliant with CMIS 5.2
- Compliant with IEEE 802.3db
- Compliant to IEEE 802.3ck
- Less than 14W in temperature range of 0 to 70℃

Applications

- 800GBASE-SR8 800G Ethernet
- Data center

Ordering Information

Part Number	Data Rate (Gb/s)	Wavelength (nm)	Transmission Distance(m)	Fiber Type	DDMI	Connector	Temperature (℃)
UFQ8HSR8	850	860	100m	MMF	YES	MPO 1x16 APC	0℃~+70℃

Note:

1. OM4 fiber, 60m for OM3 fiber
2. Case Temperature after assembling

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Ts	-40	85	℃
Case Operating Temperature	Top	0	70	℃
Relative Humidity (non-condensation)	RH	15	85	%

Supply Voltage	Vcc	-0.5	3.6	V
Receiver Damage Threshold, per Lane	PRdmg	5		dBm

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Top	0	70	℃
Relative Humidity(non-condensing)	RH	15	85	%
Power Supply Voltage	Vcc	3.135	3.465	V
Total Power Consumption	Pc	-	14	W
Supply Current per end			4.465	A
Bit Rate	BR		850	Gbps
Fiber Length on OM3 MMF			60	m
Fiber Length on OM4 MMF			100	m
I2C Clock Frequency	0		400	kHz

Electrical Characteristics

Parameters	Min	Typical	Max	Unit
Pre FEC Bit Error Ratio			2.4E-4	
Post FEC Bit Error Ratio			1E-12	
Transmitter (each Lane)				
Differential pk-pk Input Voltage tolerance	750			mV
Differential Termination Mismatch			10	%
Eye height	10			mV
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G–1)			dB
Vertical eye closure			12	dB
Effective return loss	7.3			dB
Transition Time	10			ps
Receiver (each Lane)				
Differential data output swing	300		900	mVpp
Differential termination mismatch			10	%
Eye height	15			mV

Vertical eye closure			12	dB
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G–1)			
Effective return loss	8.5			dB
Transition time	8.5			ps

Optical Characteristics

Transmitter Optical Interface

Parameter		Symbol	Min	Typical	Max	Unit
Data rate per lane		DR		53.125		GBd
Modulation format			PAM4			
Center Wavelength [1]		λ	840	860	868	nm
RMS spectral width		σ			0.6	nm
Average Launch power, each lane		P_{avg}	-4.6		4	dBm
Optical Power OMA, each Lane，max		P_{OMA}	3.5			dBm
OMAouter, each lane min	max (TECQ, TDECQ) <1.8 dB		max [-2.6 , max(TECQ,TECQ) – 4.4]			dBm
	1.8 < max (TECQ, TDECQ) < 4.4 dB					
Transmitter and dispersion eye closure (TDECQ), each lane		TDECQ			4.4	dB
Transmitter eye closure for PAM4 (TECQ), each lane		TECQ			4.4	dB
Extinction ratio		ER	2.5			dB
Transmitter power excursion, each lane					2.3	dBm
Optical Return Loss Tolerance		ORLT			14	dB
Optical Power for TX DISABLE					-30	dBm
Encircled fluxb[2]			⩾86% at 19 um ⩽30% at 4.5 um			

Receiver Optical Interface

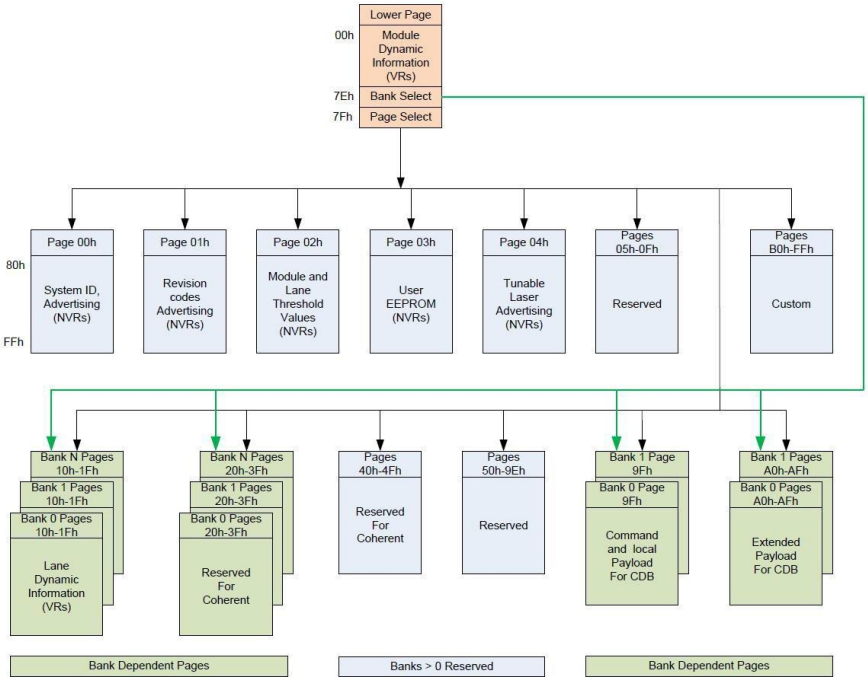
Parameter	Symbol	Min	Typical	Max	Unit
Data rate per lane	BR		53.125		Gbd
Modulation format		PAM4			
Center Wavelength	λ	842	850	948	nm
Damage threshold		5			dBm
Average receive power, each lane		–6.4		4	dBm
Receive power, each lane (OMAouter)				3.5	dBm
Receiver reflectance	Rr			–15	dB

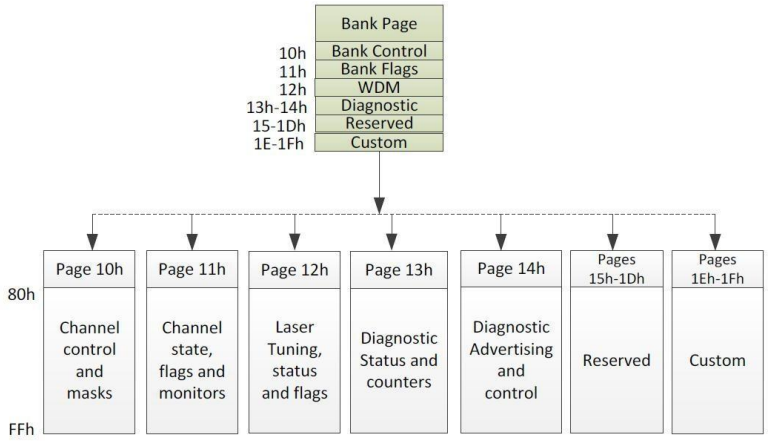
Receiver sensitivity, each lane[1]			RS = max (-4.6 , TECQ – 6.4)			dBm
Stressed receiver sensitivity, each lane					–2	dBm
Rx LOS	Assert		-15			dBm
	De-assert				-7.5	dBm
	Hysteresis		0.5		5	dB

Note:

1. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

Management Interface





Multiple Applications Support

The UFQ8HSR8 supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

Application Advertising

Address (Dec)	Application		Value (Hex)	Description
	AppSel Code	Name		
85	NA	Module Type encoding	1	Optical Interfaces: MMF
86	0001b	HostInterfaceID	4B	HostInterfaceIDApp1:100GAUI-1-S C2M
87		MediaInterfaceID	D	MediaInterfaceIDApp1:100GBASE-SR
88		HostLaneCount&MediaLaneCount	11	LaneCountApp1： TX & RX 1 lanes
89		HostLaneAssignmentOptions	FF	Permissible first host lane number: lanes 1, 2, 3, 4, 5, 6, 7, 8
01h:176		MediaLaneAssignmentOptions	FF	Permissible first media lane number: lanes 1, 2, 3, 4, 5, 6, 7, 8
90	0010b	HostInterfaceID	11	HostInterfaceIDApp2:400GAUI-8
91		MediaInterfaceID	10	MediaInterfaceIDApp2:400GBASE-SR8
92		HostLaneCount&MediaLaneCount	88	LaneCountApp2:TX & RX 8 lanes
93		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:177		MediaLaneAssignmentOptions	1	Permissible first media lane numbern: lane 1
94	0011b	HostInterfaceID	E	HostInterfaceIDApp3:200GAUI-8 C2M
95		MediaInterfaceID	0	MediaInterfaceIDApp3:200GBASE-SR8(SFF-8024 Undefined)
96		HostLaneCount&MediaLaneCount	88	LaneCountApp3:TX & RX 8 lanes
97		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:178		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
98	0100b	HostInterfaceID	51	HostInterfaceIDApp4:800G S C2M
99		MediaInterfaceID	12	MediaInterfaceIDApp4:800G-SR8
100		HostLaneCount&MediaLaneCount	88	LaneCountApp4:TX & RX 8 lanes
101		HostLaneAssignmentOptions	1	HostLaneAssignmentOptionsApp4:begin lane 1
01h:179		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
102	0101b	HostInterfaceID	4F	HostInterfaceIDApp5:400GAUI-4-S C2M
103		MediaInterfaceID	11	MediaInterfaceIDApp5:400GBASE-SR4
104		HostLaneCount&MediaLaneCount	44	LaneCountApp5:TX & RX 4 lanes
105		HostLaneAssignmentOptions	11	Permissible first host lane number: lane 1, 5
01h:180		MediaLaneAssignmentOptions	11	Permissible first media lane number: lane 1,5
106	0110b	HostInterfaceID	4D	HostInterfaceIDApp6:200GAUI-2-S C2M
107		MediaInterfaceID	1B	MediaInterfaceIDApp6:200GBASE-SR2
108		HostLaneCount&MediaLaneCount	22	LaneCountApp6： TX & RX 2 lanes
109		HostLaneAssignmentOptions	55	Permissible first host lane number: lanes 1, 3, 5, and 7
01h:181		MediaLaneAssignmentOptions	55	Permissible first media lane number: lanes 1, 3, 5, and 7
110			FF	HostInterfaceIDApp7
111			0	MediaInterfaceIDApp7
112			0	LaneCountApp7
113			0	HostLaneAssignmentOptionsApp7
114			0	HostInterfaceIDApp8
115			0	MediaInterfaceIDApp8
116			0	LaneCountApp8
117			0	HostLaneAssignmentOptionsApp8

As shown in the table above，the UFQ8HSR8 supports 6 applications, 800GBASE-SR8, 400GBASE-SR8,200GBASE-SR8,2X400GBASE-SR4,4X200GBASE-SR2,and 8X100GBASE-SR1.

Application Selection and Instantiation

The host can select Applications by programming the AppSel value in Staged Set 0. AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.

*Note that the channels of the module are independent and can be configured separately.(ie. up to eight 100GBASE-SR instances can be configured), however, it does not support different applications with different channels at the same time

UFQ8HSR8 supports two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized，which is simpler.

First mothod:

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appsel. Write application configuration to DPConfigLane<i> in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation. The Active Set can be read from page11h.

For example, select AppDescriptor3:

Step 1: Write 0x30 in Page10h Byte145~Byte152(8 bytes)—Set AppselCode3

Step 2: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

Second mothod:

Set the value of Page10h Byte240. This is a private definition.

Private Host Electrical Interface Codes

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	100GAUI-1-S C2M	100GBASE-SR1
1	00000001b	400GAUI-8	400GBASE-SR8
2	00000010b	200GAUI-8	200GBASE-SR8
3	00000011b	800G S C2M	800G-SR8

4	00000100b	400GAUI-4-S C2M	400GBASE-SR4
5	00000101b	200GAUI-2-S C2M	200GBASE-SR2

TX & RX Squelch

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported.

TX input equalization

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

RX output Equalization

RX output Equalization follows CMIS Table 6-7, with default 1dB, readable and writable

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	**Reserved**	**Reserved**
11-15	1011b-1111b	Custom	Custom

QSFP-DD Rx Output Equalization code table

RX output amplitude

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to-peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	**Reserved**
15	1111b	Custom

QSFP-DD Rx Output Amplitude code table

Loopback capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

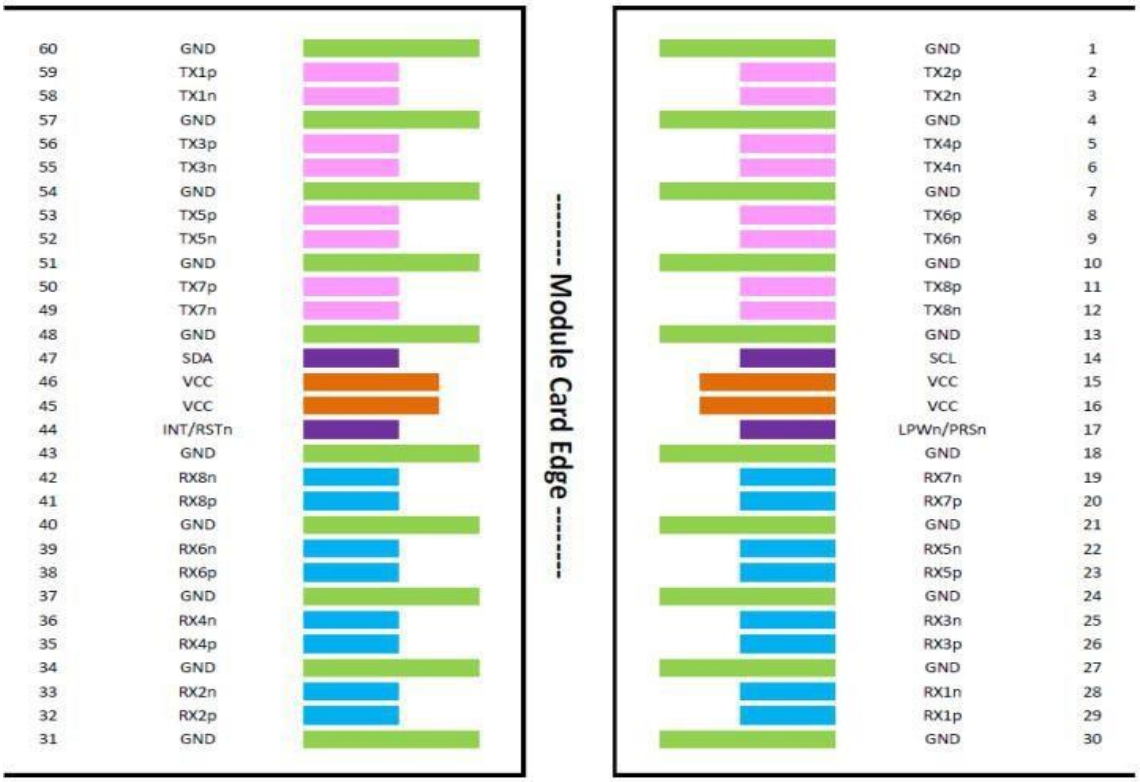
Parameter	Accuracy	Unit
Internally measured transceiver temperature[1]	+/-3	℃
Internally measured transceiver supply voltage	+/-3	%
Measured Tx bias current	+/-10	%
Measured Tx output power[2]	+/-3	dB
Measured Rx received average optical power	+/-3	dB

Notes:

1. Test point is the hotspot of the module.
2. DDM reports stability within 0.5 dB when temperature is stable. TX DDM reportes -40 dBm when TX disable

PIN Definitions

OSFP Transceiver Pad Layout, host PCB OSFP Pinout, and PIN Descriptions are as follows:



OSFP Transceiver Electrical Pad Layout

Pin Description

Pin	Name	Logic	Description	Plug Sequence	Notes
1	GND		Ground	1	
2	Tx2p	CML-I	Receiver Data Non-Inverted	3	
3	Tx2n	CML-I	Receiver Data Inverted	3	
4	GND		Ground	1	
5	Tx4p	CML-I	Receiver Data Non-Inverted	3	
6	Tx4n	CML-I	Receiver Data Inverted	3	
7	GND		Ground	1	
8	Tx6p	CML-I	Receiver Data Non-Inverted	3	
9	Tx6n	CML-I	Receiver Data Inverted	3	
10	GND		Ground	1	
11	TX8p	CML-I	Receiver Data Non-Inverted	3	
12	TX8n	CML-I	Receiver Data Inverted	3	
13	GND		Ground	1	
14	SCL	LVCMOS-I/O	2-wire Serial interface clock	3	

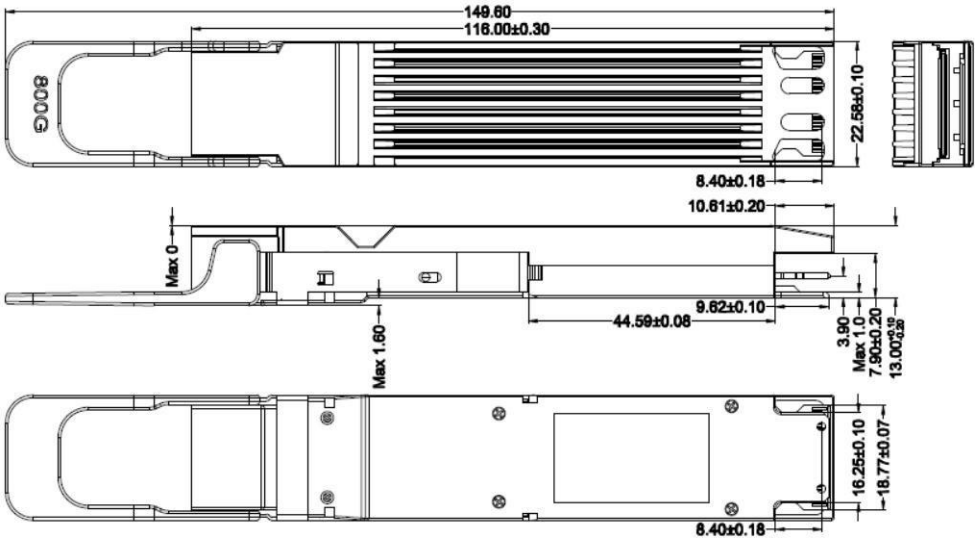
15	VCC		+3.3V Power	2	
16	VCC		+3.3V Power	2	
17	LPWn/PRSn	Multi-Level	Low-Power Mode / Module Present	3	1A
18	GND		Ground	1	
19	RX7n	CML-O	Receiver Data Inverted	3	
20	RX7p	CML-O	Receiver Data Non-Inverted	3	
21	GND		Ground	1	
22	RX5n	CML-O	Receiver Data Inverted	3	
23	RX5p	CML-O	Receiver Data Non-Inverted	3	
24	GND		Ground	1	
25	RX3n	CML-O	Receiver Data Inverted	3	
26	RX3p	CML-O	Receiver Data Non-Inverted	3	
27	GND		Ground	1	
28	RX1n	CML-O	Receiver Data Inverted	3	
29	RX1p	CML-O	Receiver Data Non-Inverted	3	
30	GND		Ground	1	
31	GND		Ground	1	
32	RX2p	CML-O	Receiver Data Non-Inverted	3	
33	RX2n	CML-O	Receiver Data Inverted	3	
34	GND		Ground	1	
35	RX4p	CML-O	Receiver Data Non-Inverted	3	
36	RX4n	CML-O	Receiver Data Inverted	3	
37	GND		Ground	1	
38	RX6p	CML-O	Receiver Data Non-Inverted	3	
39	RX6n	CML-O	Receiver Data Inverted	3	
40	GND		Ground	1	
41	RX8p	CML-O	Receiver Data Non-Inverted	3	
42	RX8n	CML-O	Receiver Data Inverted	3	
43	GND		Ground	1	
44	INT/RSTn	Multi-Level	Module Interrupt / Module Reset	3	1B
45	VCC		+3.3V Power	2	
46	VCC		+3.3V Power	2	
47	SDA	LVCMOS-I/O	2-wire Serial interface data	3	

48	GND		Ground	1	
49	TX7n	CML-I	Transmitter Data Inverted	3	
50	TX7p	CML-I	Transmitter Data Non-Inverted	3	
51	GND		Ground	1	
52	TX5n	CML-I	Transmitter Data Inverted	3	
53	TX5p	CML-I	Transmitter Data Non-Inverted	3	
54	GND		Ground	1	
55	TX3n	CML-I	Transmitter Data Inverted	3	
56	TX3p	CML-I	Transmitter Data Non-Inverted	3	
57	GND		Ground	1	
58	TX1n	CML-I	Transmitter Data Inverted	3	
59	TX1p	CML-I	Transmitter Data Non-Inverted	3	
60	GND		Ground	1	

Notes:

1. Plug Sequence specifies the mating sequence of the host connector and module. The contact sequence is1,2,3.
2. LPWn/PRSn is a Multi-level signal for low power control from host to module and module presence indication from module to host. It designed according to OSFP Module Specification Section 13.5.3
3. INT/RSTn is a Multi-level signal for interrupt request from module to host and reset control from host to module. It designed according to OSFP Module Specification Section 13.5.2

Mechanical Dimensions

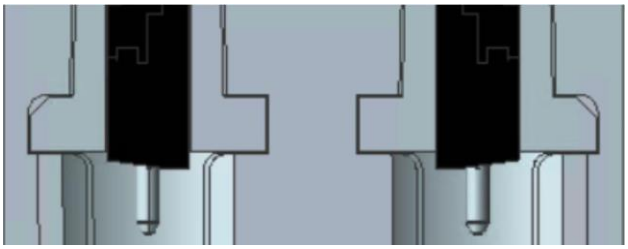


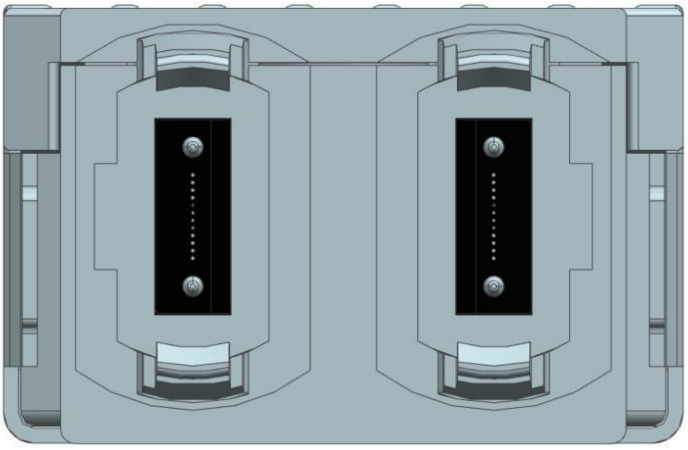
Pull-tab Color

Dual MPO12 Module appearance

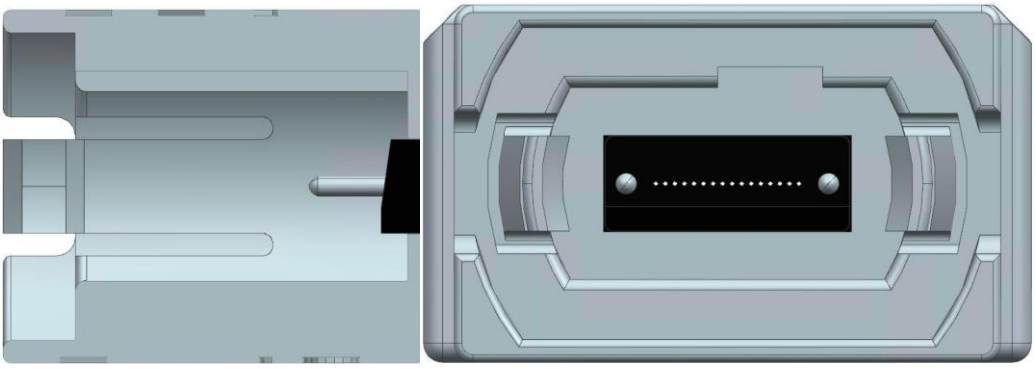
MPO16 Module appearance

Optical interface requirement





Dual MPO12 APC interface



Male MPO APC connector and MPO 16 fiber lane assignments

Laser safety and Electromagnetic Compatibility

Laser safety

The UFQ8HSR8 are Class 1 Laser products according to FDA/CDRH、IEC-60825-1 and IEC60825-2 standards. They must be operated under the specified operating conditions

Revision History

Revision	Notes	Authors	Checked	Approval	Date
SHAPE	original version	XuJian	ZhuYunguan	ZhuGuangyu	2022.04.08